

## Announcement

# Z CIRCUIT ENHANCES ZCHAR EMBEDDED MEMORY CHARACTERIZATION FLOW

***ZChar All-in-one characterization system provides  
fast turn-around time and ease-of-use for memory characterization***

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Z Circuit Automation, Inc., a leader in cell library design tools, today announced Numonyx B.V. has deployed ZChar all-in-one library characterization system for instance-based memory characterization. ZChar is used at Numonyx for all library characterization projects. Custom memory characterization in particular had been a difficult problem to solve and ZChar is able to provide a unique and efficient solution.

“We tried several approaches for memory characterization and all of them encountered unacceptable problems with scalability, usability, and accuracy.” said Thomas Parker, R&D Manager For Basic Collateral at Numonyx. “Using ZChar with Synopsys CustomSim for simulation, resulted in very accurate memory models in a fraction of the time and effort than I originally expected.”

## **Advanced Memory Models Critical For Digital Design Teams**

Memory characterization is essential to the success of integrated circuits; however, with the increase of complexity in cell models, memory characterization model quality and accuracy have not kept pace. Characterization of memory instances is a far more difficult and run-time demanding task than characterization of even the most complex standard cells.

In many chips, timing paths related to memories are the most critical paths in the system and are often associated with high fan outs and long interconnect lines, the situations that benefit the most from the highly accurate current source models, such as Synopsys CCS and Cadence ECSM models. In addition, many designs today are multi-voltage System-on-Chip (SOC) designs with a wider range of components and memories than previous generation IC designs.

## **Embedded Memory Characterization Background**

Embedded memories are created either from a memory generator or designed as custom memories. Generated memories are typically characterized in a few incremental sizes from specially generated circuit files. This characterized data stored in a special database is used to produce estimated performance models for any size generated memory within the range of the characterized data set. However, estimated models suffer from a loss of accuracy and significant margin has to be added in. It can also be difficult to quickly re-characterize a memory model estimator to special conditions, new operating voltages, or to estimate advanced models such as current source models.

Better accuracy and flexibility is achieved using instance-based characterization of the memory. In addition, all custom memories require instance-based characterization.

## **Simpler Memory Characterization Flows**

“Memory instance characterization has traditionally been a complex task because memory models require complex pin/bus representations, complex simulations, and memories are very large as compared to standard cells.” notes Fred Obermeier, Ph.D., Z Circuit co-founder and CTO. “This task becomes even more complex in lieu of folded memories, dual-port memories with multiple clocks, and many other architecture variations that require a versatile memory model generation system. We’ve architected ZChar as a general-purpose characterization system, so that all advanced model generation capabilities for timing, noise and power, are applicable to any circuits, including memories, IO pads, analog and custom blocks. Special pre-analysis capabilities allow ZChar to operate in a push-button mode even on large, complex memories. Our users have also experienced that a well-designed, all-in-one system provides other benefits including knowledge sharing, resource sharing, efficiency, and consistent, reproducible results.”

Characterization problems are magnified with memories because of the scalability issues in working with memory instances with thousands or millions of transistors. Generating special path circuits or cutting a donut from a memory instance are traditional methods to speed up simulation time. However, when static circuit reduction can be avoided or minimized, it greatly simplifies the task and risk of error for the user. For many cases, reduction is not required when using both a very fast simulator, such as Synopsys CustomSim, and a very fast characterization system, such as Z Circuit’s ZChar characterization system.

However, ZChar has now enhanced the flow by using multiple integrated methodologies to both reduce extraction time and produce reduced netlists that reliably represent critical memory models. This results in a more than 10X reduction in memory characterization runtimes and greater flexibility for the user.

## **Unmatched Simulator Integration**

ZChar is integrated with major commercial circuit simulators from Z Circuits partners Synopsys, Cadence, and Mentor as well as several internal customer simulators. Users may employ different simulators for different parts of the same memory depending on their requirements for accuracy, performance, and resources. This type of flexibility is critical in many situations to achieve a high quality result in a reasonable timeframe.

Fully extracted memory designs with hundreds of thousands of transistors have been accurately and completely characterized in less than one hour using ZChar-MS with Synopsys CustomSim running in a parallel flow. Even with a single license, runtimes are in hours due to Z Circuits very fast characterization methods and CustomSim’s efficiency with extracted memory circuits.

## About Z Circuit

Z Circuit supplies high-end cell library characterization and validation tools to some of the largest semiconductor design companies in the world. Z Circuit is privately held. To request further information or demonstration, please call Z Circuit at (650)559-1714.

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