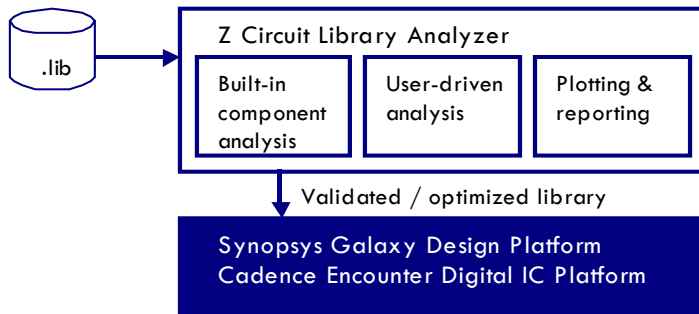


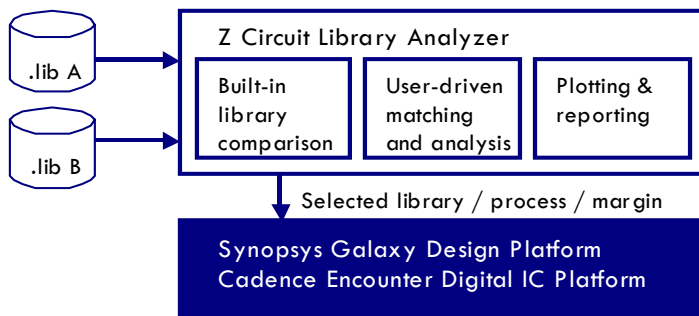
Library Analyzer

Compare and Validate Cell Libraries

Library validation and optimization flow



Library, process and release qualification flow



Z Circuit Library Analyzer, the industry-leading library analysis tool, lets design engineers and library qualification teams compare and validate complex ASIC cell libraries for characteristics that can make or break a design, such as performance, area, and power. If your team qualifies libraries from an external supplier or develops library models internally, Library Analyzer is a critical library analysis and verification tool for ensuring high-quality libraries in your design flow.

Qualify Libraries

Before a design begins, a library qualification team must decide on a foundry, library vendor, technology, feature size, and library version. While there are macro issues to consider, such as process availability, yield, and corporate relationships, there are also critical performance issues to

consider. Z Circuit Library Analyzer lets library qualification teams make well-informed decisions by giving them quantitative data as well as a graphical representation of the differences between libraries.

Z Circuit's matching technology emulates design implementation speed/area trade-offs when evaluating libraries and processes. A library qualification team can then quickly evaluate libraries across a wide range of operating conditions without the long delays of running hundreds of full chip design flows.

Validate Library Quality

With over 1 million data points per library, manual comparisons or evaluations are not feasible. Models for 65nm and below have become increasingly complex including state-dependence, noise, power, and

BENEFITS

Qualify libraries or processes:

- Select the best match
- Evaluate effects of process change on an existing design

Validate library quality:

- Reduce costly design delays
- Avoid tape-out delays

Set margins with greater knowledge:

- Improve risk/reward trade-off
- Understand performance across PVT to properly set sign-off requirements

Improve design results:

- Eliminate or fix poor performers
- Quickly perform what-if analysis for new components
- Optimize new components

FEATURE SUMMARY

Capabilities:

- Compare libraries to verify correctness or evaluate performance
- Direct check libraries to rules
- Automatically find cell maps between libraries based on cell behavior
- Query, report and graph results between any number of libraries at once

Supports:

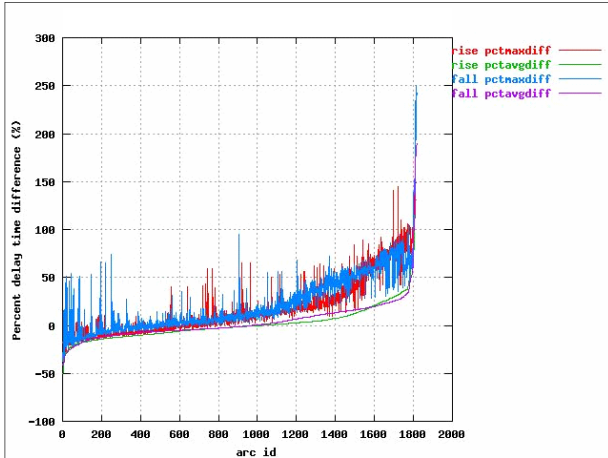
- Complete Synopsys Liberty format
- All components: standard cells, memories, I/O, custom components
- All models: timing, power, noise
- All data: NLD, CCS, all attributes

Ease-of-use:

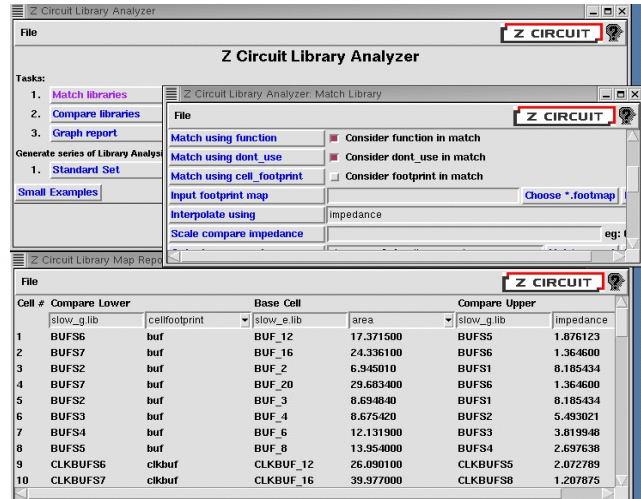
- Built-in, automated analysis flows
- Graphical and command-line
- Direct spreadsheet and plotting

Design Environment Flows:

- Synopsys, Cadence, Mentor and others



Z Circuit Library Analyzer can compare two libraries to assess differences in performance, power, or area. Results show overall relative performance and identify poorly behaved components. This graph shows a comparison of about 1800 delay arcs, approximately 88,200 points.



Z Circuit Library Analyzer provides an interactive GUI for rapid exploration of library information. Advanced mapping capabilities support comparisons over a wide variety of libraries.

inconsistent indexes. Ensuing problems may not be detected until as late as failure analysis for a failed design. Leading-edge design teams understand that early validation of complex building blocks saves them from costly delays and results in higher performance and more efficient designs with better correlation to silicon.

Evaluate Changes / Set Margins

Design engineers use Z Circuit Library Analyzer to learn how process changes affect their libraries and how library changes influence their designs. They find out which cells get faster or slower, and by how much. Evaluating effects of process change on setup and hold times for an existing design allows engineers to quickly determine what additional sign-off checks are required.

Designers also evaluate libraries across operating conditions and special sign-off corners to determine how components track across PVT. This information is essential in improving the risk/reward trade-off for setting margins and operating conditions. Library developers tune existing compo-

nents and compare new cells against existing ones to learn if changes are as expected. They also use Z Circuit Library Analyzer for quality assurance, checking to see that new library releases do not have any unexpected characteristics.

Improve Design Results

Design engineers will often choose to remove or add components to the library to improve performance. Design objectives, including performance, area, and power.

Z Circuit Library Analyzer identifies poor performers and provides a component generation capability that allow designers to perform what-if analysis for new component candidates.

Understand Release Updates

Commercial library vendors may issue frequent library updates, some are optional; others are mandatory. Z Circuit Library Analyzer lets design teams compare a new library release with its previous so that the new releases can be qualified or rejected quickly, during a design cycle.

Easy to Use

Z Circuit Library Analyzer is used in either an automatic, non-graphical command-line mode or through an advanced, interactive GUI for rapid exploration of the library information.

Query and Report

Z Circuit Library Analyzer has an optional query/report system that reports and/or graphs any data in any number of libraries.

From The Library Experts

Z Circuit offers Library Analyzer, ZChar Library Characterization, and other library development products. The Z Circuit team has extensive experience in design methodologies and library characterization.

For further information, please visit our website at www.z-circuit.com or call us at (650) 559-1714 to start an evaluation.



Z Circuit Automation, Inc.
 809 Cuesta Drive B-2210
 Mountain View, CA 94040
 650.559.1714
www.z-circuit.com