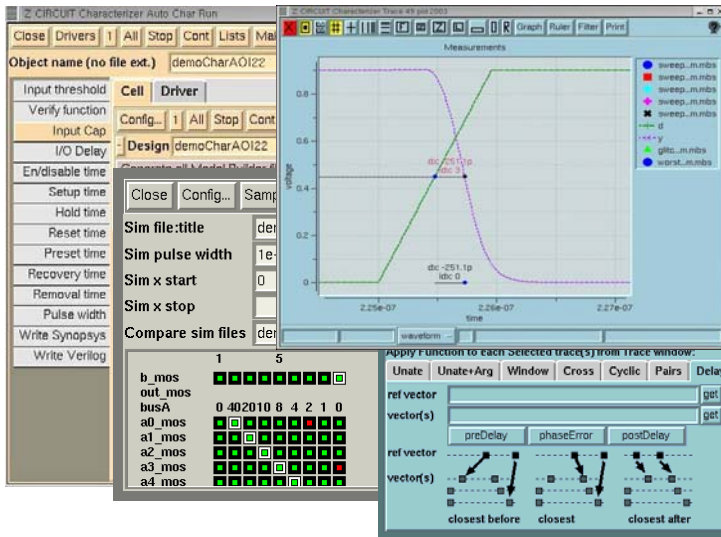


ZChar

High-Throughput Cell Library Characterization



Characterize an entire library in days instead of weeks with ZChar's highly efficient, parallel algorithms. Optimize and debug complex circuits in minutes with ZChar's unique, graphical, single-step mode and integrated waveform analysis.

ZChar quickly produces accurate performance models for standard cells, I/O's, memories, and complex cells within an advanced, integrated environment. Characterize timing, power, and noise for design platforms such as Synopsys Galaxy and Cadence Encounter Digital IC Platform.

Auto-import and characterize existing libraries to account for changes in process models, cell layouts, spice models, voltage thresholds, or for a special voltage requirement. Without correctly characterized libraries, an entire design project and millions of dollars in design and fabrication time may be at risk. Designing at the wrong environmental corner or not taking advantage of a special operating voltage, may lead to a slower, larger design that wastes power or takes much longer to close timing.

High Throughput

ZChar's advanced algorithms and efficient job distribution reduces characterization time from weeks to days, when compared to many internal and commercial systems. Complex flip-flops that would normally take 30 minutes to complete on a single machine, can finish in as little as 1 minute.

During characterization, spice simulations are continuously monitored. Numerous data checks and recovery mechanisms significantly improve turn-around time by pinpointing specific model results and simulations, if a problem is detected.

Accurate Models

At 65 nanometer and below, speed and power consumption are much more sensitive to environmental conditions including voltage and noise. Therefore, producing accurate models at the appropriate conditions is critical to achieving design success.

ZChar quickly generates accurate and complete timing/power models and incorporates unique methods for noise immunity and signal integrity to avoid design problems that otherwise might not be detected until failure analysis. Accurate timing models are created using correct input patterns and realistic waveforms.

Memory and IO Pad Models

ZChar has a very customizable modeling environment that gives complete control of input stimulus and pattern sequencing. Bus pin models and pin alias provide the

BENEFITS

Build Custom Libraries:

- Any fabrication process
- Special circuits to achieve speed, power, or area advantage

Re-characterize Existing Libraries:

- Better design performance at specific operating conditions
- More accurate or complete models

FEATURES

General-Purpose: Standard Cells, Memories, IO Pads, and Macro Cells

CCS and ECSM Model Generation

Accurate Timing, Power & Noise Models

High Throughput:

- Fast turn-around time (TAT) for both combinational and sequential cells
- Efficient batch environment structure and multi-simulation job control

Accurate, Reliable Models:

- Automatic input pattern generation for worst-case patterns
- Waveform glitch detection
- State-dependent timing, power, and leakage models.
- Override control for special cases such as differential inputs, illegal input states, and more

Ease of Use:

- Automatic import of cells from .lib or cell specification
- Formal circuit recognition methods
- Automatic configuration of tables
- Match an existing library

Advanced Interfaces:

- Interfaces with **Library Analyzer** for library validation and reporting
- Interfaces with Synopsys **HSPICE**, **HSIM**, Cadence **Spectre**, Mentor **ELDO**, and many other simulators.

versatility to create precise memory and IO Pad libraries with all required worst-case representations.

Because ZChar is a general-purpose model system, advanced models such as CCS and ECSM can be created for any circuits including memories.

Advanced Power Models

Liberty advanced power models for level shifters and other power control methods are supported.

State-Dependent Models

A versatile state-dependent specification system creates state-dependent models for timing and power. State-dependent leakage includes automatic state generation.

CCS and ECSM Models

An option for building Synopsys CCS or Cadence ECSM models is available. This next-generation technology enables improved timing accuracy and power models, especially critical for 90 nanometer and below technologies.

Noise Models for SI Analysis

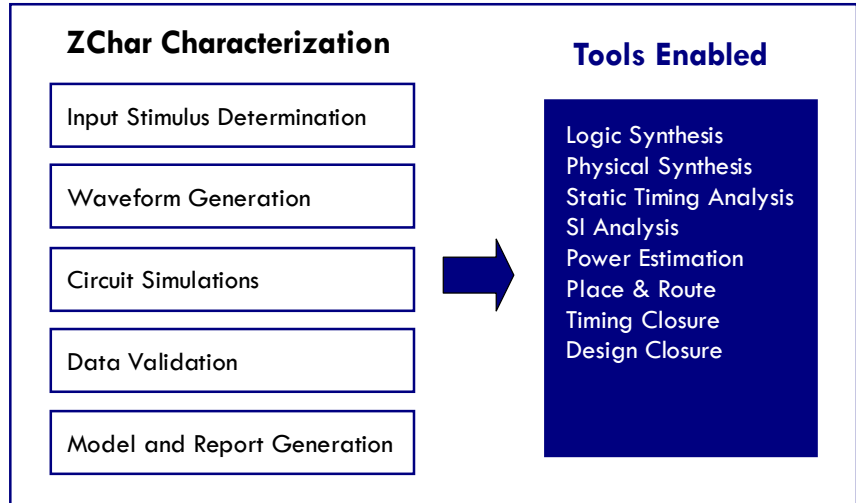
An option for building Synopsys Liberty noise models creates noise immunity and propagation data. Integration and generation of CCS-noise models are also provided.

Integrated Environment

An integrated waveform viewing environment allows users to rapidly identify problems in circuit behavior and works with all supported simulators. This environment also provides a true, real-time view into the object-oriented library configuration.

Automated Configuration

Configure ZChar quickly and easily by importing an existing library or with ZChar's unique inheritable object methodology. Advanced automated pattern generation and load determination provides highly accurate and precise models.



Rapid implementation and deployment of digital design libraries with Z Circuit ZChar is achieved with automatic input stimulus determination, versatile waveform generation, and an efficient hierarchical property database. A batch, distributed processing flow is performed with built-in job distribution.

ZChar uses formal mapping methods when importing cells and provides extensive examples for modeling complex sequential and other storage components.

Validation and Reporting

Check data completeness against expected results and cross-checks library views with built-in validation utilities.

Datasheet and Front-end Views

Produce html or PDF datasheets from user-customizable TCL templates with the ZChar datasheet generator. User-specific report or dynamic web-query can be created. Generate and validate Verilog, Vital, and VHDL front-end views.

Versatile Interfaces

ZChar creates efficient SPICE runs with Synopsys HSPICE, Cadence Spectre, Mentor Eldo, and Berkeley Spice (BSIM3 and BSIM4 models), and can be integrated with internal simulators. Users can easily switch between different simulators within the

same setup environment and obtain consistent final results for consistent simulators.

Use Library Analyzer to compare the effects of spice model changes, layout changes, and optimizing cell performance. Validate characterized libraries against previous library versions and/or against provided golden models.

From The Library Experts

The Z Circuit team has extensive experience in design methodologies and library characterization. Design services and consulting are available to assist you in getting your library development environment in place quickly.

All Z Circuit tools run on Solaris, Linux, and other UNIX-based platforms. For further information about ZChar, Library Analyzer, or other Z Circuit tools or services, please visit our website at www.z-circuit.com or call us at (650) 559-1714.



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